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1. (Once Amended) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer,

wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to be a step form having a part extending in the first direction.

823-7  
A2

8. (Once Amended) A smart card, comprising:

a ROM;

a CPU using a runnable program fixed at the time of the manufacture of a component in the ROM; and

a RAM, which enables the CPU to enter and use temporary data during its operation, wherein

the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, the conductive line partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines.

823-7  
A3

10. (Once Amended) A smart card according to claim 8, wherein

the conductive line is shaped so as to pass across the bit lines two or more times.

823-7  
A4

14. (Once Amended) A smart card, comprising:

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a ROM;

a CPU using a runnable program fixed at the time of the manufacture of a component in the ROM; and

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a RAM, which enables the CPU to enter and use temporary data during its operation, wherein

the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, wherein the conductive line is shaped to be a step form partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines two or more times.

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17. (Once Amended) A method according to claim 15, wherein the conductive line is shaped so as to pass across the bit lines two or more times.

3. Please add the following claims:

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21. (Newly Added) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

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a conductive line arranged in a second layer, located above the first layer, wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to pass across the bit lines two or more times.

22. (Newly Added) A semiconductor integrated circuit according to claim 21, wherein the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

23. (Newly Added) A semiconductor integrated circuit according to claim 21, wherein the conductive line has two ends both extending toward the same side of a ROM block.

## II. In the Specification

1. Please amend the specification as follows:

**Please replace the paragraph on page 1, line 1, that begins "The present invention..." with the following paragraph:**

The present invention relates to small size cards, such as smart cards and chip cards; and more particularly, to a design of conductive lines arranged over bit lines of a ROM block.

**Please replace the paragraph on page 6, line 8 that begins "Fig. 3 is circuitry..." with the following paragraph:**

Fig. 3 is a circuitry layout 102 in a smart card according to a first embodiment of the present invention. A ROM includes bit lines 104 arranged to extend in a first direction, which is a vertical in the figure. The bit lines 104 are formed in a first layer. In a second layer located above the first layer, conductive lines 106 are formed to extend in a second direction, which is orthogonal to the first direction. Each of the conductive

AA lines 106 is shaped to be a step form so as to across the bit lines 104 as much as possible and to improve the degree of freedom of circuitry design. In other words, the conductive lines 106 can extend in any direction at the ends, so that the semiconductor integrated circuit can be designed without a lot of restrictions.

**Please replace the paragraph on page 7, line 12, that begins "Fig. 4 is another circuitry..." with the following paragraph:**

AA Fig. 4 is another circuitry layout in a smart card according to a second embodiment of the present invention. A ROM includes bit lines 204 arranged to extend in a first direction, which is a vertical in the figure. The bit lines 204 are formed in a first layer. In a second layer located above the first layer, conductive lines 206 are formed to extend in a second direction, which is orthogonal to the first direction. Each of the conductive lines 206 is shaped to be a step form so as to across the bit lines 204 as much as possible and to improve the degree of freedom of circuitry design. In other words, the conductive lines 206 can extend any directions at the ends, so that the semiconductor integrated circuit can be designed without a lot of restrictions.

### **III. In the Abstract of the Disclosure**

**Please replace the Abstract with the following paragraph:**

AA A semiconductor integrated circuit includes a ROM having bit lines extending in a first direction in a first layer. A conductive line is arranged in a second layer above the first layer, extending in a second direction, which is orthogonal to the first direction, across the bit lines. The conductive line is shaped to be a step form having a part